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Television waveform monitoring arrangement

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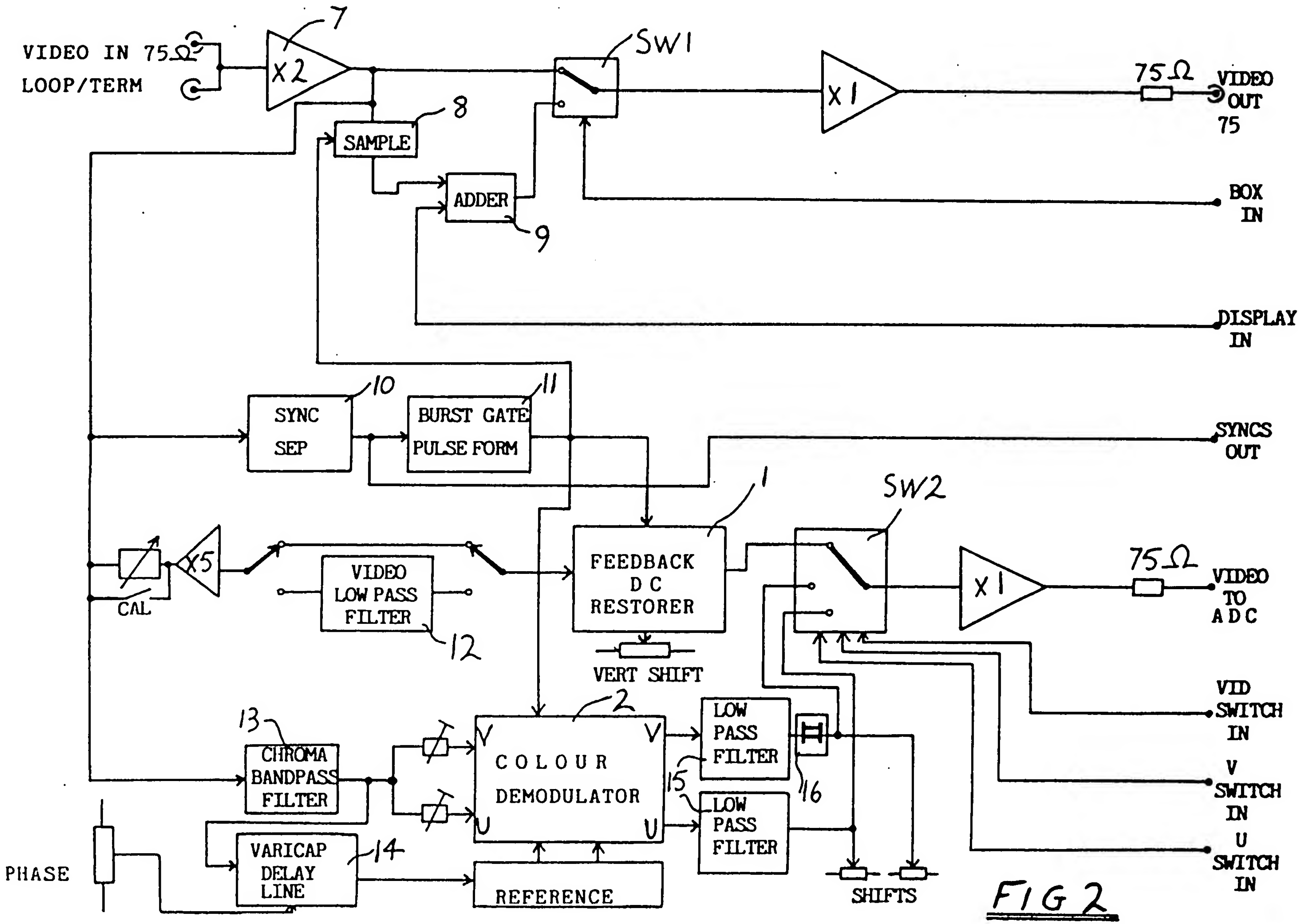

VIDEO IN 75Ω
LOOP/TERM
X2
7
SW1
X1
75Ω
VIDEO OUT 75
SAMPLE
8
ADDER
9
BOX IN
DISPLAY IN
SYNC SEP
10
BURST GATE PULSE FORM
11
SYNCS OUT
1
SW2
CAL
X5
VIDEO LOW PASS FILTER
12
FEEDBACK D C RESTORER
VERT SHIFT
X1
75Ω
VIDEO TO ADC
VID SWITCH IN
13
CHROMA BANDPASS FILTER
2
V
COLOUR DEMODULATOR
U
LOW PASS FILTER
15
16
V SWITCH IN
U SWITCH IN
PHASE
VARICAP DELAY LINE
14
REFERENCE
SHIFTS

FIG 2

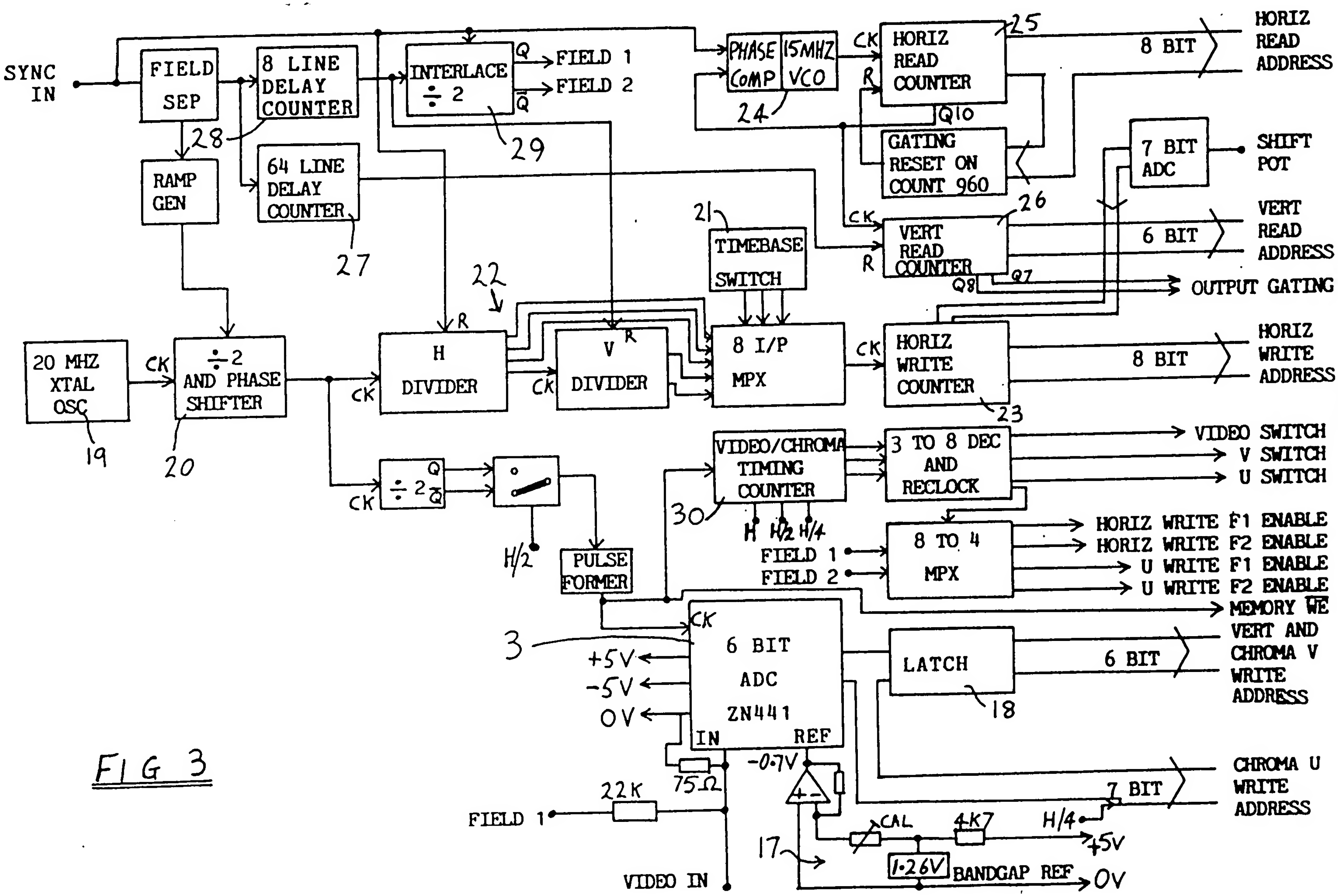

SYNC IN
FIELD SEP
8 LINE DELAY COUNTER
64 LINE DELAY COUNTER
RAMP GEN
INTERLACE ÷ 2
Q
$\bar{Q}$
FIELD 1
FIELD 2
PHASE COMP
15MHZ VCO
CK
R
HORIZ READ COUNTER
Q10
GATING RESET ON COUNT 960
8 BIT
HORIZ READ ADDRESS
7 BIT ADC
SHIFT POT
VERT READ COUNTER
Q8
Q7
6 BIT
VERT READ ADDRESS
OUTPUT GATING
TIMEBASE SWITCH
20 MHZ XTAL OSC
÷2 AND PHASE SHIFTER
H DIVIDER
V DIVIDER
8 I/P MPX
HORIZ WRITE COUNTER
8 BIT
HORIZ WRITE ADDRESS
÷ 2
VIDEO/CHROMA TIMING COUNTER
H H/2 H/4
3 TO 8 DEC AND RECLOCK
VIDEO SWITCH
V SWITCH
U SWITCH
H/2
PULSE FORMER
FIELD 1
FIELD 2
8 TO 4 MPX
HORIZ WRITE F1 ENABLE
HORIZ WRITE F2 ENABLE
U WRITE F1 ENABLE
U WRITE F2 ENABLE
MEMORY $\overline{WE}$
6 BIT ADC ZN441
IN
REF
+5V
-5V
0V
LATCH
6 BIT
VERT AND CHROMA V WRITE ADDRESS
-0.7V
75Ω
22K
FIELD 1
VIDEO IN
CAL
4K7
1·26V
BANDGAP REF
H/4
+5V
0V
7 BIT
CHROMA U WRITE ADDRESS
3
17
18
19
20
21
22
23
24
25
26
27
28
29
30

FIG 3

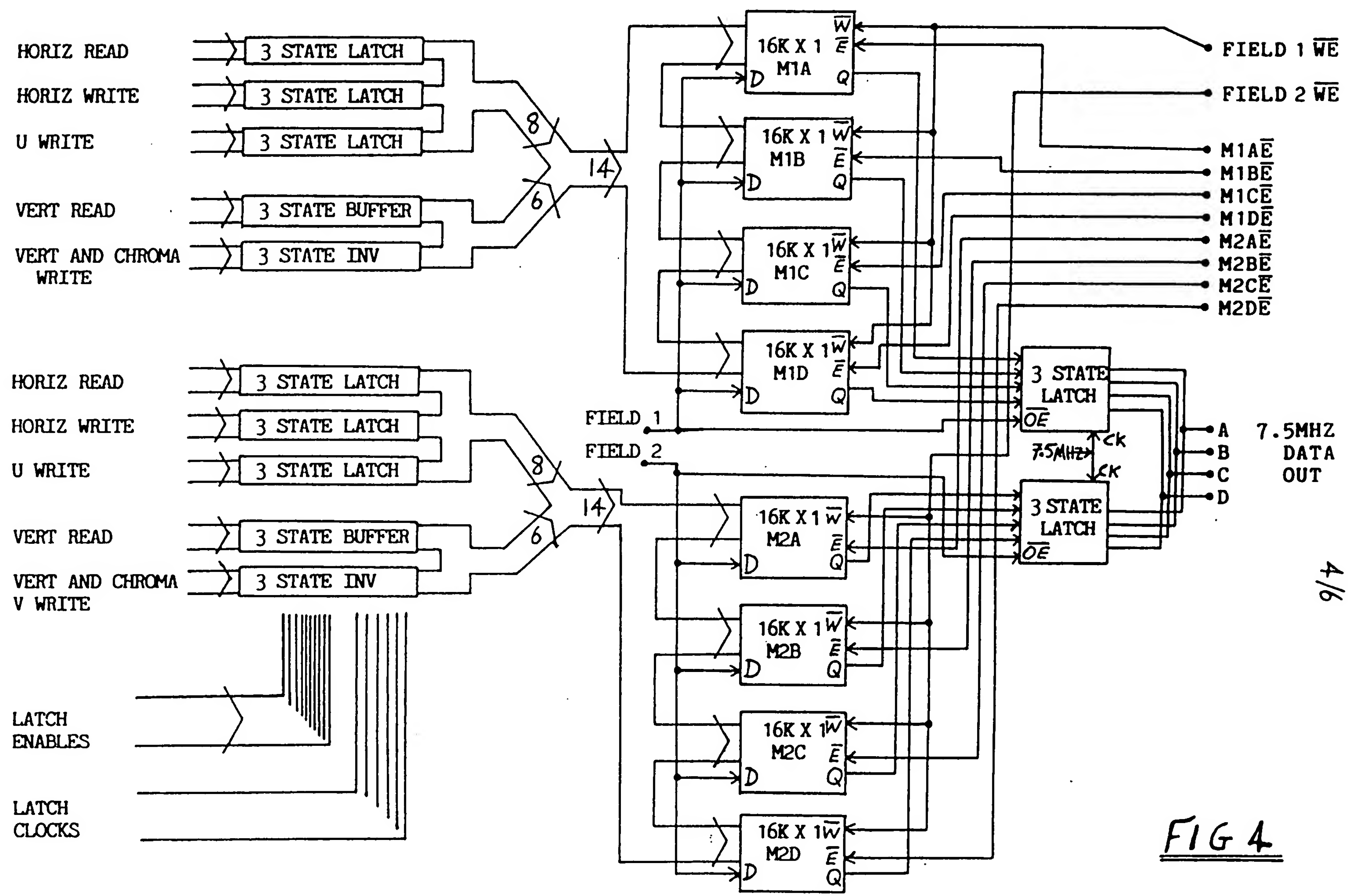

HORIZ READ
HORIZ WRITE
U WRITE
VERT READ
VERT AND CHROMA WRITE
3 STATE LATCH
3 STATE LATCH
3 STATE LATCH
3 STATE BUFFER
3 STATE INV
8
6
14
HORIZ READ
HORIZ WRITE
U WRITE
VERT READ
VERT AND CHROMA V WRITE
3 STATE LATCH
3 STATE LATCH
3 STATE LATCH
3 STATE BUFFER
3 STATE INV
8
6
14
LATCH ENABLES
LATCH CLOCKS
16K X 1 M1A
16K X 1 M1B
16K X 1 M1C
16K X 1 M1D
16K X 1 M2A
16K X 1 M2B
16K X 1 M2C
16K X 1 M2D
FIELD 1
FIELD 2
FIELD 1 WE
FIELD 2 WE
M1AE
M1BE
M1CE
M1DE
M2AE
M2BE
M2CE
M2DE
3 STATE LATCH
3 STATE LATCH
OE
CK
7.5MHz
A
B
C
D
7.5MHZ DATA OUT

FIG 4

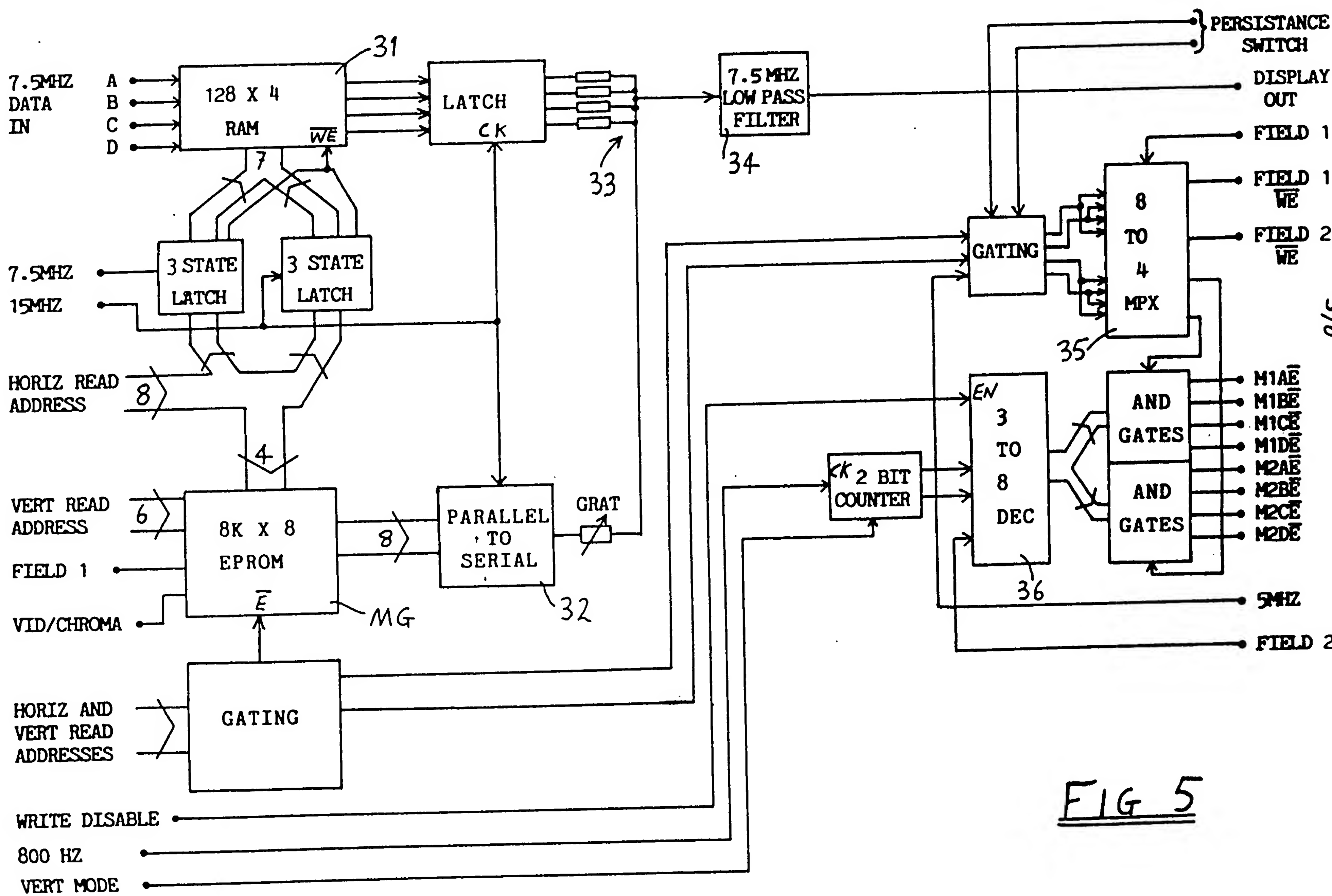
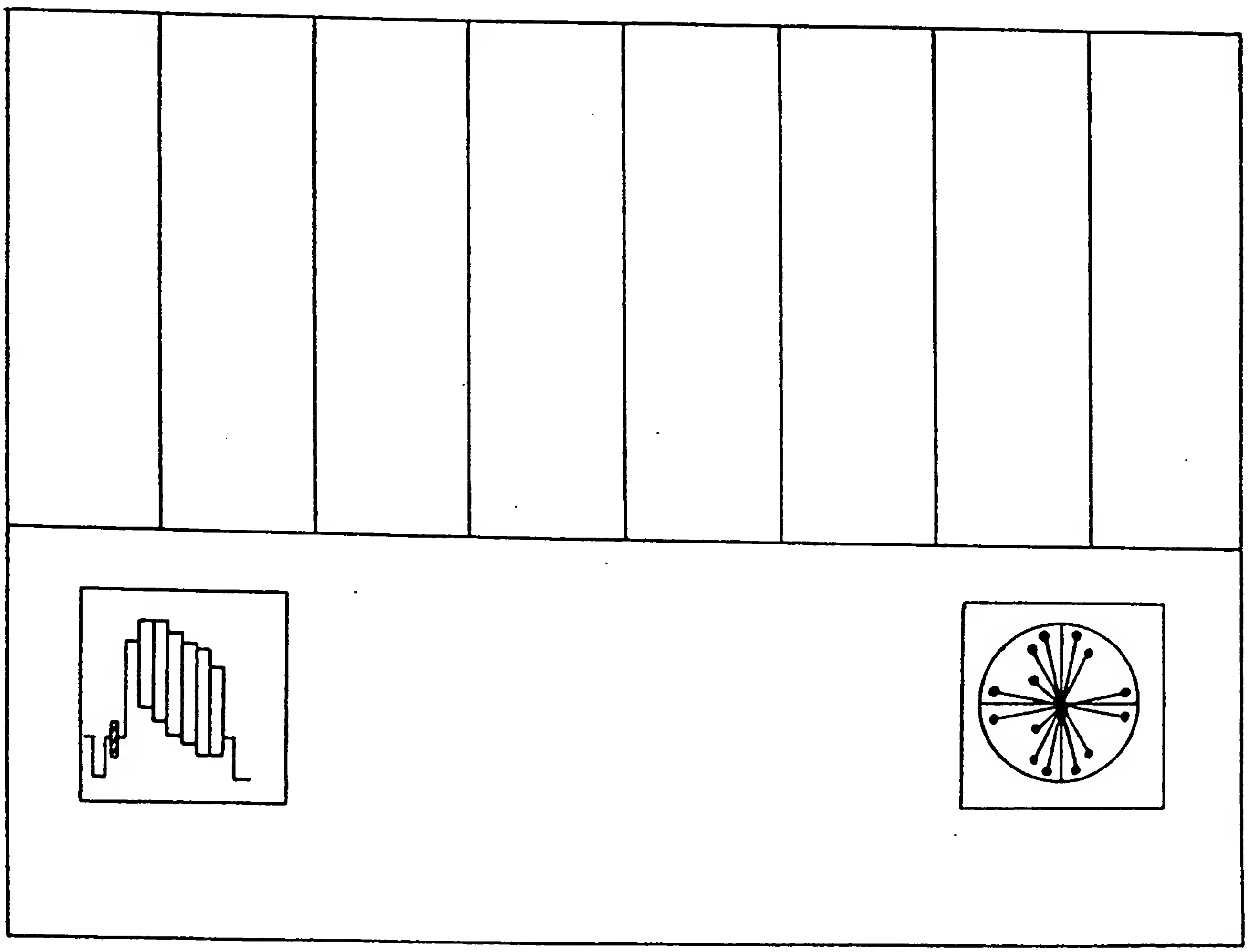

7.5MHZ DATA IN
A
B
C
D
128 X 4 RAM
WE
31
7
LATCH
CK
33
7.5 MHZ LOW PASS FILTER
34
PERSISTANCE SWITCH
DISPLAY OUT
FIELD 1
FIELD 1 WE
FIELD 2 WE
7.5MHZ
15MHZ
3 STATE LATCH
3 STATE LATCH
HORIZ READ ADDRESS
8
4
GATING
8 TO 4 MPX
35
EN
3 TO 8 DEC
36
AND GATES
AND GATES
M1AE
M1BE
M1CE
M1DE
M2AE
M2BE
M2CE
M2DE
CK 2 BIT COUNTER
VERT READ ADDRESS
6
8K X 8 EPROM
E
MG
FIELD 1
VID/CHROMA
8
PARALLEL TO SERIAL
32
GRAT
5MHZ
FIELD 2
HORIZ AND VERT READ ADDRESSES
GATING
WRITE DISABLE
800 HZ
VERT MODE

FIG 5



VIDEO

VECTOR

FIG 6

TELEVISION WAVEFORM MONITORING ARRANGEMENT

This invention relates to a system for displaying video and/or vector waveforms.

Television waveform monitors are widely used within the television industry to provide more information about the video signal than is available by observing the picture displayed on the screen. Such waveform monitors also allow technical appraisal and adjustment of the performance of the video system by analysing test signals applied to the systems. However hitherto the waveform monitors have been separate from the picture monitor, thus requiring separate C.R.T.'s and requiring the observer to move his eyes between the different screens in order to compare and appraise the picture and waveforms.

In accordance with the present invention, there is provided a television waveform monitoring system, comprising an input for receiving a video signal, an output for applying said video signal to a CRT display, means for processing said video signal and deriving therefrom video and/or vector waveform signals, and means for applying said video and/or vector waveform signals to said output for displaying said video and/or vector waveforms on the CRT display in which said processing means comprises a television field store, means for writing video and/or vector waveform signals into said television field store and means for reading said waveform signal(s) out of said store for application to said output.

Preferably the video and vector waveforms are "burnt" into the television signal (i.e. the picture itself is blacked out at the locations of the waveform displays). Preferably the system serves to display graticules to enable measurements on the waveforms to be made.

The video and vector waveforms may be displayed at the same time, preferably at different positions and for example adjacent the bottom of the screen and adjacent opposite sides. Preferably the waveform displays and the graticules are coloured differently. Facility may be incorporated into the system for varying the size of the waveform displays.

In a further development, the system may be used in conjunction with a portable television camera and serve to display either the video or vector waveform (upon selection) in the viewfinder of the camera.

An embodiment of the present invention will now be described by way of examples only and with reference to the accompanying drawings, in which:

Figure 1 is an overall block diagram of a television waveform monitoring system in accordance with this invention;

Figures 2 to 5 together form a more detailed circuit diagram of the system; and

Figure 6 is a front view of a picture monitor showng the video and vector waveforms displayed together with the picture itself.

Referring to Figure 1, a conventional 75 ohm input video signal VIDEO IN is applied to a DC restorer 1 for providing the video waveform and to a colour demodulator 2 for decoding into the U and V vectors. These signals are sampled sequentially by an analog-to-digital converter

(ADC) 3 via a switch 4: the sequence is shifted line-by-line to mask missing samples. The A.D.C. sampling clock is phase-shifted to interleave samples line-by-line, to reduce the effective sample spacing from 200 nS to 1 nS when in horizontal modes. The system further comprises a memory M, the memory address being U and V for the vector display and video and timebase counter for video display. The memory has alternate read and write fields, with each field split into four 5 mS bands, to show the relative brightness of line rate signals. The memory is read out to produce two displays VIDEO and VECTOR as shown in Figure 6, adjacent the bottom and opposite sides of the monitor screen: the data read out from the memory M is converted to analog at 5, and combined with data defining the graticule from an EPROM store MG and gated into the input video at 6 to provide the signal VIDEO OUT to be applied to the monitor.

Referring to Figure 2 to show the system in more detail, the input video is amplified x2 at 7 before being fed to the various circuits. A CMOS switch SW1 switches the output between input video and the display signal superimposed on video black level at 9. A sampler 8 serves to sample and hold on the video back porch. A conventional sync separator 10 feeds out to the logic section and also to a burst gate former 11 which forms the clamp pulse for the sampler and D.C. restorer 1 and is also the burst gate for the colour demodulator 2.

The video signal is split into two paths, the video path is applied to a switchable 1MHz low pass filter 12 before going to the D.C. restorer 1. This is of the feedback type, there the black level of the output is compared with a shift pot and the resulting error signal used to offset the input voltage. This has the advantage of not corrupting the back porch of the waveform and allows

any hum or L.F. tilt to be shown on the display.

The chroma path is applied to a 2-pole chroma bandpass filter 13 and then to a conventional colour demodulator 2 comprising a TBA540 reference chip and TBA990 demodulator, modified to disable the P.A.L. switch so that a true vector display is produced. The reference signal is applied via a 4-pole L.C. delay line 14 where the C elements are varicap diodes. By varying the D.C. to these diodes the delay of the line varies, hence providing phase rotation of the vector display. The U and V outputs from the demodulator 2 pass through 1.3MHz low pass filters 15 to remove subcarrier from them. The V waveform passes additionally through a 200nS delay line 16 because the A.D.C. samples U first and this allows the waveforms to be sampled together.

A CMOS switch SW2 selects the signal fed out and applies it to the A.D.C.3 . The switch SW2 is driven in such a way as to give 6 samples of video, then chroma U, then chroma V. Each sample has a duration of 200nS so a fast switch is needed, such as a CD4066.

Figure 3 shows circuits for the generation of the various addressed needed by the memory. Video from Figure 2 is applied to a Ferranti ZN441 6 Bit Flash A.D.C.3. The necessary reference is derived from a 1.26 volt bandgap reference circuit 17. The A.D.C. output forms the vertical video, chroma V and chroma U write addresses via a latch 18 which allows the A.D.C. output to be stored, as the following 3 state inverters have no storage. The horizontal write address is derived from a 20MHz crystal oscillator 19, which is subject to a variable phase shift and divided by 2 at 20 before being fed to the timebase divider. This is needed as in horizontal display modes the video is only sampled every 200nS and hence will not

completely sample the waveform. By phase shifting the sampling by $\pm$ 50nS and alternating the A.D.C. phase by $\pm$ 180^{o} on a line-by-line basis, over a whole field the video will be sampled every 1/2nS in effect.

A front panel timebase switch 21 controls which divider-output clocks the horizontal write counter 23. These are 10MHz for HMAG, 2MHz for H, 1MHz for 2H, 160KHz for VMAG and 6.4KHz for V (to display 1/5th of a line, 1 line, 2 lines, 1/25th of a field, or a whole field respectively).

On the read address side, a 15MHz oscillator 24 is locked by comparison of incoming line syncs with 15MHz ÷ 960 from the read counter 25, which also phases up the counter output. The vertical read counter 26 is clocked at line rate but reset on line 64 from a 64 line delay counter 27. This allows the read counter 26 to derive gating signals for the output box positions, giving output on lines 192 to 256 and erasure on lines 256 to 320. Line 320 is possible in a 312½ line frame by delaying the frame start by 8 lines, see 8 line delay counter 28. This also allows the whole field sync group to be displayed in VMAG. To synchronise the field 1/field 2 selector, line sync is gated with field sync to preset the divider 29.

The video/chroma timing counter 30 is clocked at 5MHz and is organised to provide six video samples, then chroma U, then chroma V (repeating). The control is provided by enabling the appropriate addresses to the memory.

In order to mask holes left where samples are missed, the above sequence is advanced line-by-line, by loading the counter with the 8 line delay counter on each line sync.

To provide horizontal shift of the video waveform, the horizontal write counter 23 is loaded with a word propor-

tional to a shift pot voltage over an A.D.C. 23a.

By adding a 25HZ square wave onto the VIDEO IN input to the A.D.C.3 at 1/2 L.S. bit peak-to-peak, the 6 bit converter will yield 7-bit resolution as it is offset by 1/2 its L.S. bit on the interlaced field. Similarly with chroma U where 7 bits are needed from the 6 bit converter, the L.S. bit is derived from 1/4 line rate, making sure that the chroma dots have a 1:1 aspect ratio.

Referring to Figure 4, the memory M consists of 8 identical 16K x 1 static RAMs MIA-MID and M2A-M2D, operating with 200nS cycle time in write, 133.1/3nS cycle times in read. The memory is split into alternate read and write fields to allow simultaneous reading and writing without slowing down the memory speed. Each field is split into four, each memory being equally addressed. In horizontal modes and for the chroma, the field is split into four 5ms bands, one written to each memory. This allows the frequency of occurence of line rate signals to be displayed as a variation in brightness, as with a C.R.T. display. The data input to the memory is tied high on the write plane to enter data, and tied low on the read plane to allow erasure after readout. The memory outputs are latched and the appropriate plane fed out.

Referring to Figure 5, memory data from DATA OUT of Figure 4 enters at DATA IN and is fed to a 128 x 4 static RAM 31. This is used as a speed doubler, where data is read in at 7.5MHz and out at 15MHz. This is achieved by having the read address at twice the frequency of the write address. The RAM output is converted to analog by an equally weighted D.A.C.33.

The graticule is generated in an 8K x 8 EPROM shown at MG, each graticule occupying 2K x 4 of memory, the remain-

ing 4K being spare for possible use as NTSC graticules. The EPROM output is in 8 bit blocks and is fed to a register 32 to produce 15MHz of serial data, which is added to the video waveform at 33. The combined signal passes through a 7.5MHz low pass filter 34 before being added to the video signal.

An 8 to 4 MPX at 35 is used to control which memory is fed with a write enable signal, and also to provide memory enables for readout and erasure areas. A 3 to 8 decoder 36 controls which memory is written into to provide brightness information. A front panel switch overrides the operation of the memory controller. In the STORE position writing in the read field is inhibited, stopping erasure and effectively giving infinite persistence. In the HOLD position, all writing is disabled, freezing the display.

The system which has been described thus serves to apply the video and vector displays to the video signal such that the same monitor will display the picture and the corresponding video and vector waveforms: in the example described the waveform displays are "burnt" into the video signal and a graticule is also displayed at the locations of the waveform displays. The system can include a facility for switching between P.A.L. and N.T.S.C. television systems.

CLAIMS

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1. A television waveform monitoring system, comprising an input for receiving a video signal, an output for applying said video signal to a CRT display, means for processing said video signal and deriving therefrom video and/or vector waveform signals, and means for applying said video and/or vector waveform signals to said output for displaying said video and/or vector waveforms on the CRT display, in which said processing means comprises a television field store, means for writing video and/or vector waveform signals into said television field store and means for reading said waveform signal(s) out of said store for application to said output.

2. A television waveform monitoring system as claimed in claim 1, in which said processing means is arranged to read said video and vector waveform signals of said store at appropriate timing to produce separate video and vector displays.

3. A television waveform monitoring system as claimed in claim 1 or 2, in which the video and/or vector waveforms are burnt into the picture signal being applied to the CRT.

4. A television waveform monitoring system as claimed in claim 3, in which the video and vector waveforms are displayed at the same time at different positions of the CRT display.

5. A television waveform monitoring system as claimed in any preceding claim, including means for generating and applying to said output signals providing the display of graticules against the displayed waveforms.

6. A television waveform monitoring system as claimed in claim 5, arranged for said displayed graticules and waveforms to be differently coloured.

7. A television waveform monitoring system as claimed in any preceding claim, including means for varying the size of the waveform displays.

8. A television waveform monitoring system substantially as herein described with reference to the accompanying drawings.

9. A television waveform monitoring system as claimed in any preceding claim, used in conjunction with a television camera and serving to display either the video or vector waveform in a viewfinder of the camera.